```
 * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
=> s degating or degate
            97 DEGATING
            87 DEGATE
L1         158 DEGATING OR DEGATE
=> s l1 and (electronic# or electrical)
        248432 ELECTRONIC#
        469377 ELECTRICAL

L2          59 L1 AND (ELECTRONIC# OR ELECTRICAL)
=> d ti 1-59

US PAT NO:      5,506,992 [IMAGE AVAILABLE]          L2: 1 of 59
TITLE:          Distributed processing system with asynchronous
                  communication between processing modules

US PAT NO:      5,478,517 [IMAGE AVAILABLE]          L2: 2 of 59
TITLE:          Method for molding IC chips

US PAT NO:      5,466,997 [IMAGE AVAILABLE]          L2: 3 of 59
TITLE:          Spin motor control system for a hard disk assembly

US PAT NO:      5,371,764 [IMAGE AVAILABLE]          L2: 4 of 59
TITLE:          Method and apparatus for providing an uninterrupted clock
                  signal in a data processing system

US PAT NO:      5,340,418 [IMAGE AVAILABLE]          L2: 5 of 59
TITLE:          Method for producing a cast aluminum vehicle wheel

US PAT NO:      5,336,344 [IMAGE AVAILABLE]          L2: 6 of 59
TITLE:          Method for producing a cast aluminum vehicle wheel

US PAT NO:      5,330,347 [IMAGE AVAILABLE]          L2: 7 of 59
TITLE:          Moulding press for an injection moulding device

US PAT NO:      5,328,347 [IMAGE AVAILABLE]          L2: 8 of 59
TITLE:          Device for introducing a plastic material into a mould
                  cavity

US PAT NO:      5,324,474 [IMAGE AVAILABLE]          L2: 9 of 59
TITLE:          Method of making a printed wiring board spacer

US PAT NO:      5,276,806 [IMAGE AVAILABLE]          L2: 10 of 59
TITLE:          Oblivious memory computer networking

US PAT NO:      5,258,695 [IMAGE AVAILABLE]          L2: 11 of 59
TITLE:          Spin motor control system for a hard disk assembly

US PAT NO:      5,210,855 [IMAGE AVAILABLE]          L2: 12 of 59
TITLE:          System for computer peripheral bus for allowing hot
                  extraction on insertion without disrupting adjacent
                  devices

US PAT NO:      5,150,366 [IMAGE AVAILABLE]          L2: 13 of 59
TITLE:          Reduced delay circuits for shift register latch scan
                  strings

US PAT NO:      5,099,101 [IMAGE AVAILABLE]          L2: 14 of 59
```

5,099,107

TITLE: Laser trimming system for semiconductor integrated circuit chip packages

US PAT NO: 5,095,483 [IMAGE AVAILABLE] L2: 15 of 59
TITLE: Signature analysis in physical modeling

US PAT NO: 4,978,830 [IMAGE AVAILABLE] L2: 16 of 59
TITLE: Laser trimming system for semiconductor integrated circuit chip packages

US PAT NO: 4,890,725 [IMAGE AVAILABLE] L2: 17 of 59
TITLE: Automatic continuously cycleable molding system and method

US PAT NO: 4,877,387 [IMAGE AVAILABLE] L2: 18 of 59
TITLE: Automatic continuously cycleable molding system

US PAT NO: 4,847,020 [IMAGE AVAILABLE] L2: 19 of 59
TITLE: Process of molding an optic for an intraocular lens

US PAT NO: 4,833,600 [IMAGE AVAILABLE] L2: 20 of 59
TITLE: Computer driver module for master interface to communication and control network

US PAT NO: 4,789,324 [IMAGE AVAILABLE] L2: 21 of 59
TITLE: Molded optic for an intraocular lens

US PAT NO: 4,727,477 [IMAGE AVAILABLE] L2: 22 of 59
TITLE: Logically transportable microprocessor interface control unit permitting bus transfers with different but compatible other microprocessors

US PAT NO: 4,585,152 [IMAGE AVAILABLE] L2: 23 of 59
TITLE: Method and apparatus for **degating** parts using ultrasonic energy

US PAT NO: 4,575,328 [IMAGE AVAILABLE] L2: 24 of 59
TITLE: Automatic continuously cycleable molding apparatus

US PAT NO: 4,531,165 [IMAGE AVAILABLE] L2: 25 of 59
TITLE: Automatic amplitude equalizer based upon monitoring of channel power loss

US PAT NO: 4,482,819 [IMAGE AVAILABLE] L2: 26 of 59
TITLE: Data processor system clock checking system

US PAT NO: 4,464,751 [IMAGE AVAILABLE] L2: 27 of 59
TITLE: Machine check coordination

US PAT NO: 4,460,534 [IMAGE AVAILABLE] L2: 28 of 59
TITLE: Two-shot injection molding

US PAT NO: 4,386,400 [IMAGE AVAILABLE] L2: 29 of 59
TITLE: Reset of a selected I/O channel and associated peripheral equipment by means independent of the channel

US PAT NO: 4,343,634 [IMAGE AVAILABLE] L2: 30 of 59
TITLE: Process for operating a fluidized bed

[redacted]

US PAT NO: 4,298,954 [IMAGE AVAILABLE] L2: 31 of 59
TITLE: Alternating data buffers when one buffer is empty and another buffer is variably full of data

US PAT NO: 4,273,041 [IMAGE AVAILABLE] L2: 32 of 59
TITLE: Belt printer control architecture

US PAT NO: 4,268,902 [IMAGE AVAILABLE] L2: 33 of 59
TITLE: Maintenance interface for a service processor-central processing unit computer system

US PAT NO: 4,188,665 [IMAGE AVAILABLE] L2: 34 of 59
TITLE: Programmable communications subsystem

US PAT NO: 4,171,536 [IMAGE AVAILABLE] L2: 35 of 59
TITLE: Microprocessor system

US PAT NO: 4,167,041 [IMAGE AVAILABLE] L2: 36 of 59
TITLE: Status reporting

US PAT NO: 4,156,796 [IMAGE AVAILABLE] L2: 37 of 59
TITLE: Programmable data processing communications multiplexer

US PAT NO: 4,056,843 [IMAGE AVAILABLE] L2: 38 of 59
TITLE: Data processing system having a plurality of channel processors

US PAT NO: 4,028,667 [IMAGE AVAILABLE] L2: 39 of 59
TITLE: Asynchronous, hierarchical loop communication system with independent local station control of access to inbound time portions without central control

US PAT NO: 4,020,462 [IMAGE AVAILABLE] L2: 40 of 59
TITLE: Method and apparatus for form removal from contour compressed image data

US PAT NO: 4,016,603 [IMAGE AVAILABLE] L2: 41 of 59
TITLE: Disk storage apparatus having signals recorded in a specific format

US PAT NO: 3,991,405 [IMAGE AVAILABLE] L2: 42 of 59
TITLE: Margin adjusting of textual codes in a memory

US PAT NO: 3,924,068 [IMAGE AVAILABLE] L2: 43 of 59
TITLE: Low distortion receiver for bi-level baseband PCM waveforms

US PAT NO: 3,889,241 [IMAGE AVAILABLE] L2: 44 of 59
TITLE: Shift register buffer apparatus

US PAT NO: 3,834,505 [IMAGE AVAILABLE] L2: 45 of 59
TITLE: INK JET PRINTING APPARATUS WITH LINE SWEEP AND INCREMENTAL PRINTING FACILITIES

US PAT NO: 3,829,080 [IMAGE AVAILABLE] L2: 46 of 59
TITLE: FAN-FOLDED PAPER STACKER FOR HIGH SPEED PRINTER

US PAT NO: 3,824,563 [IMAGE AVAILABLE] L2: 47 of 59

[redacted]

TITLE: DATA STORAGE TRACK PADDING APPARATUS

US PAT NO: 3,811,115 [IMAGE AVAILABLE] L2: 48 of 59
TITLE: ITEM LISTER USING A SHIFT REGISTER

US PAT NO: 3,801,962 [IMAGE AVAILABLE] L2: 49 of 59
TITLE: COMMUNICATION MECHANISM FOR DATA TRANSFER AND CONTROL BETWEEN DATA PROCESSING SYSTEMS AND SUBSYSTEMS

US PAT NO: 3,797,037 [IMAGE AVAILABLE] L2: 50 of 59
TITLE: SENTENCE ORIENTED DICTATION SYSTEM FEATURING RANDOM ACCESSING OF INFORMATION IN A PREFERRED SEQUENCE UNDER CONTROL OF STORED CODES

US PAT NO: 3,786,439 [IMAGE AVAILABLE] L2: 51 of 59
TITLE: ERROR DETECTION SYSTEMS

US PAT NO: 3,729,713 [IMAGE AVAILABLE] L2: 52 of 59
TITLE: DATA PROCESSING PERIPHERAL SUBSYSTEMS

US PAT NO: 3,720,919 [IMAGE AVAILABLE] L2: 53 of 59
TITLE: PHOTONICALLY PARTITIONED CONTINUOUS GAS ENVELOPE AND TRANSIENTLY ENERGIZED PILOT DISCHARGE AREAS USED IN ADDRESS SELECTION OF DISPLAY FIRING COORDINATES

US PAT NO: 3,713,108 [IMAGE AVAILABLE] L2: 54 of 59
TITLE: BRANCH CONTROL FOR A DIGITAL MACHINE

US PAT NO: 3,674,125 [IMAGE AVAILABLE] L2: 55 of 59
TITLE: DATA SYSTEM WITH PRINTING, COMPOSING, COMMUNICATIONS, AND MAGNETIC CARD PROCESSING FACILITIES

US PAT NO: 3,648,255 [IMAGE AVAILABLE] L2: 56 of 59
TITLE: AUXILIARY STORAGE APPARATUS

US PAT NO: 3,610,902 [IMAGE AVAILABLE] L2: 57 of 59
TITLE: **ELECTRONIC** STATISTICAL CALCULATOR AND DISPLAY SYSTEM

US PAT NO: 3,599,176 [IMAGE AVAILABLE] L2: 58 of 59
TITLE: MICROPROGRAMMED DATA PROCESSING SYSTEM UTILIZING IMPROVED STORAGE ADDRESSING MEANS

US PAT NO: 3,595,453 [IMAGE AVAILABLE] L2: 59 of 59
TITLE: METHOD OF SEPARATING PARTS USING HIGH FREQUENCY ENERGY

=>

```
=> d his
     (FILE 'USPAT' ENTERED AT 13:33:46 ON 10 APR 96)
L1            158 S DEGATING OR DEGATE
L2             59 S L1 AND (ELECTRONIC# OR ELECTRICAL)
=> s l2 and ((degate or degating) (w) (area or region or material#))
              87 DEGATE
              97 DEGATING

          732490 AREA
          341183 REGION
         1216741 MATERIAL#

               0 (DEGATE OR DEGATING) (W) (AREA OR REGION OR MATERIAL#)
L3             0 L2 AND ((DEGATE OR DEGATING) (W) (AREA OR REGION OR MATERIA
L#)
                 )
```

=> d kwic 2

US PAT NO: 5,478,517 [IMAGE AVAILABLE] L4: 2 of 59

ABSTRACT:
To . . . half is raised and ejector pins push the molded parts with it, away from the lower mold half, performing auto **degating**. The molded parts are then ejected from the upper mold half, the slide is retracted and the plastic in the. . .

SUMMARY:

BSUM(5)

After . . . metal lead frame, since the lead frame is strong and the plastic can be broken away from it during the **degating** process. However this method is not acceptable for metal coated plastic tape, since the plastic sticks to the tape and. . .

SUMMARY:

BSUM(7)

Similar difficulties have been encountered in encapsulating other **electrical** components, e.g. resistors, capacitors and diodes. The process would, for example, be faster and less costly if they could be. . .

SUMMARY:

BSUM(9)

Accordingly, . . . carrier, such that plastic will not come in contact with the carrier and so that simple part ejection with automatic **degating** can be achieved. Usually the part will be an integrated circuit chip or other **electrical** component, but it can be any appropriate part requiring encapsulation.

DETDESC:

DETD(16)

After . . . mold half 40 upwardly, retaining the encapsulated chips 12a securely in the upper mold cavity halves 54 and thereby breaking (**degating**) the encapsulated chips from the plastic in the runner system. Since the plastic in the runner system is connected to. . . mold surface 52, little force is applied to the encapsulated chips 12 a during this chip ejection procedure. Thus, automatic **degating** (i.e. removal of the parts from the plastic of the runner system) is effected.

breaking

DETDESC:

DETD(21)

It . . . also permits the plastic to be admitted into the side of the cavity, for more uniform encapsulation. In addition, auto **degating** is achieved since the part is ejected while pinning the hardened plastic in the runner system in place (by the. . .

DETDESC:

DETD(23)

While the parts being encapsulated have been described as integrated circuit chips, they can be other **electrical** components or other parts (usually small) needing encapsulation. For example, resistors or resistive networks are commonly printed on a ceramic. . .

DETDESC:

DETD(24)

Similarly . . . leads can be similarly mounted on a tape or lead frame before molding), or a combination of these or other **electrical** components. The part can also be any other small part to which fine leads or supports can be conveniently attached. . .

CLAIMS:

CLMS(2)

2. The method according to claim 1 wherein said part is an **electrical** component.

=> d kwic 8

=> d kwic 9

US PAT NO: 5,324,474 [IMAGE AVAILABLE] L4: 9 of 59

SUMMARY:

BSUM(5)

Mounts and spacers are often required to provide spacing for the **electronic** components at various elevations above PWBs. The purpose of these mounts and spacers is as follows:

SUMMARY:

BSUM(11)

An optional technique used for elevating **electronic** components of the printed wiring board is by placing a slight twist on the leads of **electronic** components. This method, commonly referred to as jog form, is labor intensive and is applicable to less than 30% of. . .

SUMMARY:

BSUM(12)

The . . . pertinent prior art of which applicant herein is aware involves wash away spacers compounded of organic material (lactose) for spacing **electronic** components on printed wiring boards. The manufacturing technique of these spacers is unknown. Prior to flow/wave solder processing, the wash away spacers of various shapes and desired thickness are placed between **electronic** components and the printed wiring board to raise the **electronic** component height to a desired elevation. Most often the leads of the **electronic** components pass through the spacers inside diameter and finally through printed wiring board to keep spacer intact between the **electronic** component and the printed wiring board during flow solder process. The spacers can also be placed between **electronic** components and printed wiring board without leads passing therethrough to provide desired spacing between **electronic** components and the printed wiring board. These techniques can be expensive since lactose spacers are brittle, difficult to handle and. . .

SUMMARY:

BSUM(22)

The . . . very brittle. Tumbling of the runner system while liquid nitrogen is being sprayed thereon or immediately thereafter, causes parts to **degate** from the remainder of the runner system, breaking away at brittled thin gate sections. Parts can then be easily separated. . .

SUMMARY:

BSUM(23)

As an alternate **degating** technique, the spacers can be automatically degated during molding operation by utilizing a subgate (tunnel gate).

SUMMARY:

9 of 59

BSUM(24)

In either technique the remainder of the runner system after **degating** the part can be pelletized and recycled into the molding process.

DETDESC:

DETD(9)

The . . . configuration 21 or sections of runner system 23 while liquid nitrogen is being sprayed or immediately thereafter, causes parts to **degate** from the sub-runner system 28, breaking away at brittled thin gate sections. Spacers 27 can then be easily separated from. . . a room temperature to prevent any condensation of moisture on the just degated spacers 27 using liquid nitrogen as the **degating** technique.

DETDESC:

DETD(10)

As an alternate **degating** technique, the spacers 27 can be automatically degated during the molding operation by utilizing a sub-gate (tunnel gate).

=> d ab 9

US PAT NO: 5,324,474 [IMAGE AVAILABLE] L4: 9 of 59

ABSTRACT:
Thermoplastic printed wiring board spacers are fabricated by providing a water soluble partially hydrolyzed polyvinyl alcohol resin or fully hydrolyzed polyvinyl alcohol resin or a blend of partially hydrolyzed polyvinyl alcohol resin and fully hydrolyzed polyvinyl alcohol resin, the ration thereof depending upon (1) the degree of hydrolyzation of the polyvinyl alcohol resins, (2) crystallinity associated with particular polyvinyl alcohol resins, (3) the fabrication temperatures of the printed wiring board to avoid spacer melting and (4) the degree of solubility in water of the spacer. The spacers are fabricated by injection molding the polyvinyl alcohol resins or desired polyvinyl alcohol resin mixture to provide a molded configuration having a runner system with spacers attached to a sub runner system by a very thin gate. The spacers are removed from the molded configuration by initially cooling the surface of the total molded configuration to a temperature at which the thin gate sections becomes very brittle. The cooled molded configuration is then subjected to tumbling or a jolt whereby the spacers break away from the runner system at the gates.

=>

=> d kwic 14

US PAT NO: 5,099,101 [IMAGE AVAILABLE] L4: 14 of 59

ABSTRACT:
An automatic laser trimming apparatus (30) for semiconductor integrated chip packages removes dambars (16) and performs deflashing and **degating** operations. The apparatus combines a laser machining subsystem (32, 36) with a machine vision subsystem (38, 40) to accurately locate. . .

SUMMARY:

BSUM(2)

The . . . packages. The system is specifically designed for the fully automatic precision removal of dambars as well as the deflashing and **degating** of semiconductor lead frame packages.

SUMMARY:

BSUM(30)

After the dambars are removed and the deflashing and **degating** steps are completed, the fixture is opened and the material handling system moves the completed piece out of the fixture. . .

DETDESC:

DETD(12)

The galvanometers convert **electrical** current information into mechanical energy via shaft rotation. Accordingly, the mirror rotation of the galvanometer system is controlled by varying. . .

DETDESC:

DETD(31)

In addition to the dambar removal and deflashing operation, the subject system also performs a **degating** operation. In the **degating** operation, the connection between the gate 12 and the die 13 is broken. Since this step also consists of plastic. . . is performed with the defocusing lens 54 in place. When all of the dambars are removed, and the deflashing and **degating** operations are completed, a package as shown in FIG. 2 is produced. As can be seen, the conductive leads 15. . .

DETDESC:

DETD(32)

In . . . semiconductor integrated chip packages. The system is designed for the precision removal of dambars as well as the deflashing and **degating** of semiconductor lead frame packages. The system combines a laser machining subsystem with a machine vision subsystem to accurately locate. . .
=>

```
=> s (4954308 or 5241133 or 5270262 or 5185653 or 4490902 or 4043027)/pn
             1 4954308/PN
             1 5241133/PN
             1 5270262/PN
             1 5185653/PN
             1 4490902/PN
             1 4043027/PN
L5           6 (4954308 OR 5241133 OR 5270262 OR 5185653 OR 4490902 OR 404
302
               7)/PN
=> s l5 and (degating or deflashing)
            97 DEGATING
           246 DEFLASHING
L6           0 L5 AND (DEGATING OR DEFLASHING)
=> s l5 and (breaking)
         83014 BREAKING
L7           1 L5 AND (BREAKING)
=> d kwic
US PAT NO:      **4,043,027** [IMAGE AVAILABLE]          L7: 1 of 1

DETDESC:

DETD(7)

 With . . . dies 60 and 62, displacement of the conductor wire is held
to an absolute minimum so that the likelihood of **breaking** the whisker
leads 52 or 54 is held to a minimum.
=> save l5 rd0410a/a
ANSWER SET 'L5' HAS BEEN SAVED AS 'RD0410A/A'
=>
```

[redacted]